



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/683,836

02/21/2002

James A. Bruce

BUR920010049

9685

29625

7590

12/08/2005

MCGUIRE WOODS LLP

1750 TYSONS BLVD.

SUITE 1800

MCLEAN, VA 22102-4215

EXAMINER

STREGE, JOHN B

ART UNIT

PAPER NUMBER

2625

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/683,836

Applicant(s)

BRUCE ET AL

Examiner

John B. Strege

Art Unit

2625

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 and 36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 and 36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☒ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/12/05 has been entered.

***Withdrawal of the Restriction***

The claims have been amended so that they now have the same limitations as the non-traversed restricted subject matter. As it is no longer a burden on the Examiner the previous restriction is now withdrawn, and the inventions I and II are rejoined.

***Response to Arguments***

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-2,4-5,8,11-20 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cai et al. USPN 6,873,720 (hereinafter "Cai") in view of Aloni et al. USPN 6,366,687 (hereinafter "Aloni").

Cai discloses a method of evaluating the effect of defects on components in a semiconductor manufacturing process (component is read as an integrated circuit mask, col. 1 lines 6-7), said method comprising the steps of: inspecting a component for defects using an inspection tool (as seen in figure 5 the physical mask 501A has a defect detection processor 504); recording defect inspection data from the inspection tool (storage device 508); accessing design data from a reference mask (501B); modifying said design data for the component according to said defect inspection data (a simulated wafer image is formed in numeral 511 based on the reference mask and the defect data, here simulation is read as modifying); analyzing said modified design data (defect printability analysis generator 515); Cai further discloses identifying critical and non-critical regions of the integrated circuit (514, col. 14 lines 49-61, and col. 8 lines 45-67) and using this information in addition to the simulated data in the defect printability analysis generator 515 to characterize (classify) the defects as substantial or unsubstantial (critical or non-critical, col. 9 lines 3-8); and determining a final disposition of the component by applying different acceptance rules to the critical defects and the non-critical defects (paragraph bridging cols. 17-18, col. 5 lines 22-58, here tolerances are read as the different acceptance rules, depending on the criticality of the region the tolerance levels used for the severity score are different paragraph bridging cols. 14-15).

Cai does not explicitly disclose that the design data comes from a design data repository, however it is well known in image processing to store design data in a database. Aloni discloses an optical inspection system used for inspecting masks or the chips or wafers constructed with such masks that uses a database containing design data corresponding to a reference.

Cai and Aloni are analogous art because they are both from the same field of endeavor of mask inspection. At the time of the invention it would have been obvious to one of ordinary skill in the art to obtain the reference data from a database. The motivation for doing so is that a database could hold different types of reference data thus allowing for inspection of different masks. Thus it would have been obvious to one of ordinary skill in the art to combine Cai and Aloni to obtain the invention as specified in claim 1.

Regarding claim 2, as discussed Cai discloses that the invention is for mask inspection.

Regarding claims 4-5, Cai discloses that the final disposition of the mask being inspected includes scrapping the mask, repairing the mask, or accepting the mask and determining whether a defect is likely to cause failure (paragraph bridging cols. 17-18).

Regarding claim 8, as discussed Cai does not disclose a database for the reference data however it would be obvious to do so. Furthermore it would be obvious to use the storage device 508 to store the reference data. The database 508 includes a computer hard disk drive, a CD ROM, and a server, all of which are capable of storing large files.

Claim 11 has the same limitations as claims 1-2, thus the same arguments used for claims 1-2 apply equally to claim 11.

Claim 12-14 are similarly analyzed as claim 4.

Regarding claim 15, Cai discloses using heuristic rules to determine if the defect will be resolved onto the wafer (col. 13 lines 25-67).

Claims 16-18 are similar to claims 11-13 except claims 16-18 are system claims thus they are similarly analyzed and rejected.

Claims 19-20 are similar to claims 11-12 except claims 19-20 are computer readable medium claims, thus they are similarly analyzed and rejected.

Claim 36 is similar to claim 1 thus it is similarly analyzed and rejected.

3. Claims 3,6, and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cai et al. USPN 6,873,720 (hereinafter "Cai") in view of Aloni et al. USPN 6,366,687 (hereinafter "Aloni") and further in view of Chang et al. USPN 6,757,645 (hereinafter "Chang").

Regarding claims 3 and 6, Cai discloses determining the size and location of a defect, but does not explicitly disclose designating the defect type as opaque or clear. However Cai incorporates by reference application number 09/130,996 (now the Chang patent). Chang discloses that the mask compromises opaque areas and clear areas (col. 2 lines 20-38) and that a defect printing depends greatly on its location, size, and transmission/reflection characteristics (col. 4 lines 10-29). Thus it would be obvious to

include if the defect is clear or opaque with the defect data to determine the importance of that part of the mask.

Cai and Chang are analogous art because Chang is incorporated by reference into Cai. Thus it would have been obvious to one of ordinary skill in the art to include whether the defect data is clear or opaque since it is an important characteristic of the defect. Thus it would have been obvious to one of ordinary skill in the art to combine Cai, Chang, and Aloni to obtain the invention as specified in claim 3.

Regarding claim 9, the design image simulator of Cai is incorporated by reference from the Chang patent (col. 12 lines 55-67). Chang discloses that the design image simulator 960 simulates a defect shape for the mask layer being inspected corresponding to defects from said defect detection processor 925.

Regarding claim 10, Chang discloses that different mask layers are used to produce the semiconductor device with various layers and shows an effective method for inspecting a layer of the mask. Chang nor Cai explicitly disclose analyzing both intra-level and inter-level problems of the mask layer, but it would be obvious to do so in order to accurately determine the defects of the mask which are important with respect to the desired representation of the photo-resist material etched into the silicon (Chang, col. 3 lines 39-61).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cai et al. USPN 6,873,720 (hereinafter "Cai") in view of Aloni et al. USPN 6,366,687 (hereinafter

"Aloni") in view of Chang et al. USPN 6,757,645 (hereinafter "Chang"), and further in view of Mansfield et al. USPN 5,965,306 (hereinafter "Mansfield").

Chang discloses creating a simulated wafer image of a defect 970 and merging the image into a simulated wafer image (as seen by 2030 of figure 20. Chang does not explicitly disclose that the defect inspection data comprises intensity contour plots.

It is well known in the art of mask inspection to use the inspection tool AIMS which produces intensity contour plots.

Mansfield discloses that a standard mask inspection/repair process entails incorporating the defect size criterion of the device manufacture into the inspection tool and that advanced mask maker may utilize the AIMS tool to facilitate this process (col. 4 lines 30-46).

Cai, Aloni, Mansfield and Chang are all analogous art because they are from the same field of endeavor of mask inspection.

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine Cai, Aloni, Mansfield and Chang to use the AIMS inspection tool thus producing intensity contour plots in order to facilitate the inspection process. Thus it would have been obvious to combine Cai, Aloni, Mansfield and Chang to obtain the invention of claim 7.

#### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Strege whose telephone number is (571) 272-




Art Unit: 2625

7457. The examiner can normally be reached on Monday-Friday between the hours of 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS

  
BHAVESH M. MEHTA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600